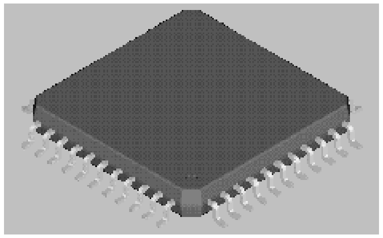
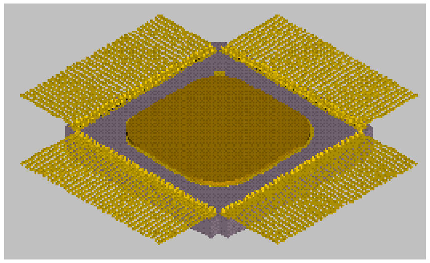
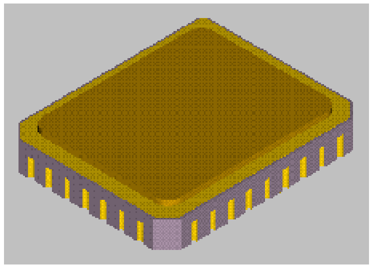
Digital Component

- Plastic Quad Flat Package (PQFP)

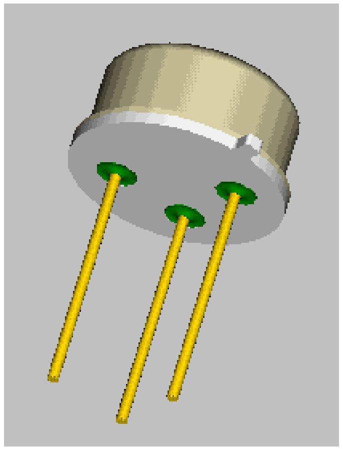


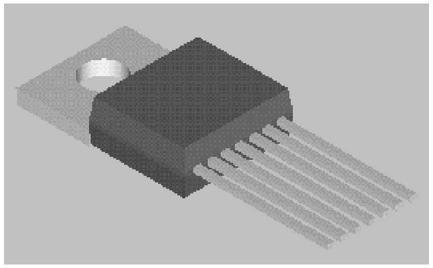


- Ceramic Leadless Chip Carrier (LCC)



- TO Packages (Transistor single Outline)





2-2 Decoder / Encoder

- Decoder
  - A combinational circuit that converts binary information from the ***n*** coded inputs to a maximum of 2^n unique outputs
  - ***n***-to-***m*** line decoder = ***n x m*** decoder
    - ***n*** inputs, ***m*** outputs
  - If the n-bit coded information has unused bit combinations, the decoder may have less than 2^n outputs
    - $m \leq 2^n$
- 3-to-8 Decoder
  - Logic Diagram : ***Fig. 2-1***
  - Truth Table : ***Tab. 2-1***
  - Commercial decoders

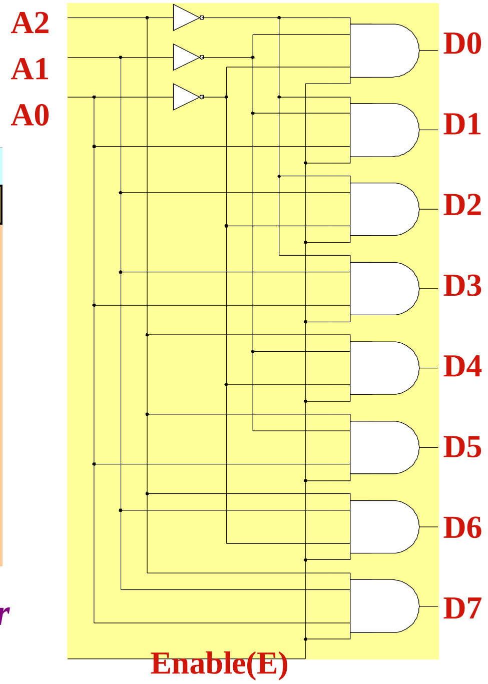
    include one or more

    Enable Input(E)

Enable	Inputs			Outputs							
E	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Tab. 2-1 Truth table for 3-to-8 Decoder

Fig. 2-1 3-to-8 Decoder



- NAND Gate Decoder

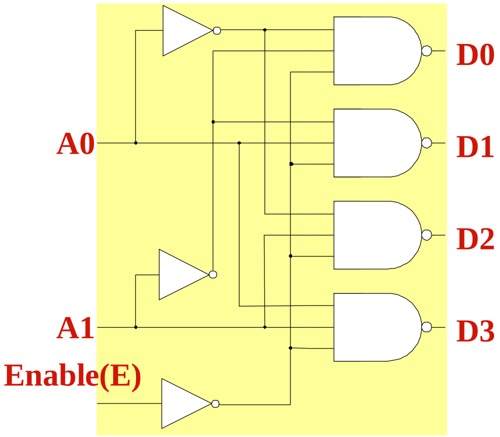
  * Active Low Output
  * Fig. 2-1 3-to-8 Decoder Active High Output

  - Constructed with NAND instead of AND gates
  - Logic Diagram/Truth Table : ***Fig. 2-2***

Fig. 2-2 2-to-4 Decoder with NAND gates

Enable	Input		Output			
E	A1	A0	D3	D2	D1	D0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

(a) Truth Table



(b) Logic Diagram

- Decoder Expansion
  - 3 X 8 Decoder constructed with two 2 X 4 Decoder
  - Constructed decoder : ***Fig. 2-3***

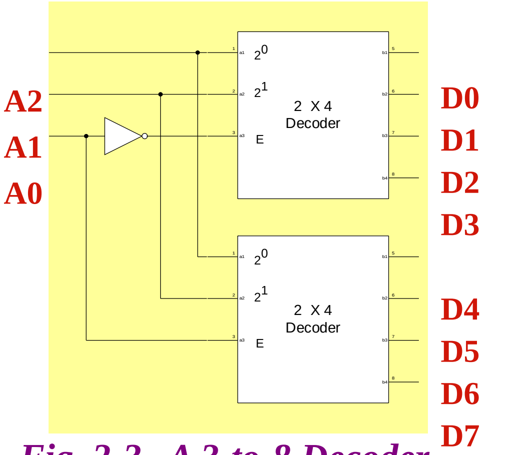


Fig. 2-3 A 3-to-8 Decoder constructed with two with 2-to-4 Decoder

- Encoder
  - Inverse Operation of a decoder
  - 2^n input, n output
  - Truth Table : ***Tab. 2-2***
    - 3 OR Gates Implementation
      - » A0 = D1 + D3 + D5 + D7
      - » A1 = D2 + D3 + D6 + D7
      - » A2 = D4 + D5 + D6 + D7

Tab. 2-2 Truth Table for Encoder

Inputs								Outputs		
D7	D6	D5	D4	D3	D2	D1	D0	A2	A1	A0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

2-3 Multiplexers

- Multiplexer(Mux)
  - A combinational circuit that receives binary information from one of 2^n input data lines and directs it to a single output line
  - A 2^n -to 1 multiplexer has *2^n input data lines* and *n input selection lines*(Data Selector)
  - 4-to-1 multiplexer Diagram : ***Fig. 2-4***
  - 4-to-1 multiplexer Function Table : ***Tab. 2-3***

Tab. 2-3 Function Table for 4-to-1 line Multiplexter

Select		Output
S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

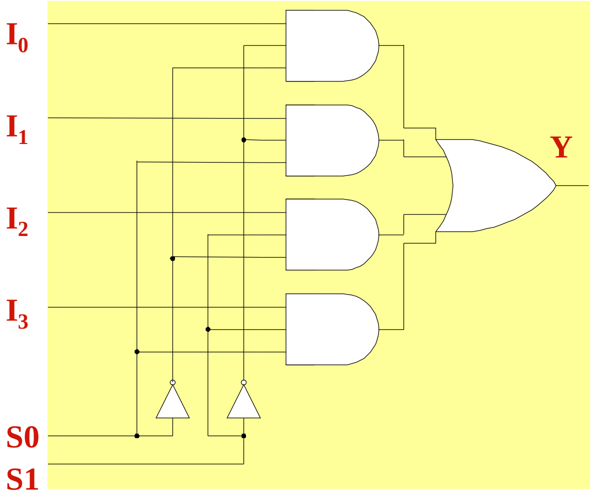


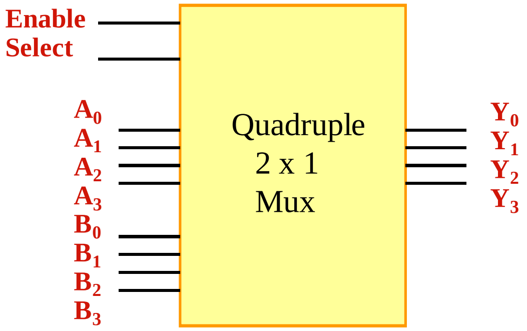
Fig. 2-4 4-to-1 Line Multiplexer

- Quadruple 2-to-1 Multiplexer
  - Quadruple 2-to-1 Multiplexer : ***Fig. 2-5***

Fig. 2-5 Quadruple 2-to-1 line Multiplexter

Select		Output
E	S	Y
0	0	All 0's
1	0	A
1	1	B

(a) Function Table



(b) Block Diagram

2-4 Registers

- Register
  - A group of flip-flops with each flip-flop capable of storing one bit of information
  - An n-bit register has a group of n flip-flops and is capable of storing any binary information of n bits
  - The simplest register consists only of flip-flops, with no external gate : ***Fig. 2-6***
  - A clock input C will load all four inputs in parallel
    - The clock must be *inhibited* if the content of the register must be left unchanged
- Register with Parallel Load
  - A 4-bit register with a load control input : ***Fig. 2-7***
  - The clock inputs receive clock pulses at all times
  - The buffer gate in the clock input will increase "fan-out"
  - Load Input
    - 1 : Four input transfer
    - 0 : Input inhibited, Feedback from output to input(***no change***)

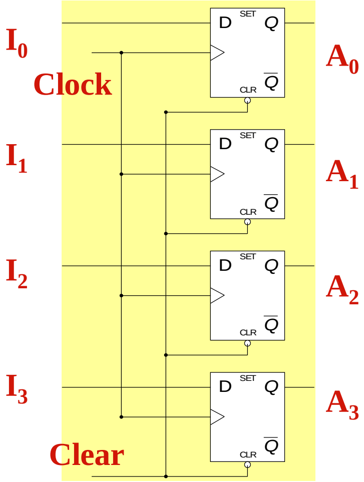


Fig. 2-6 4-bit register

2-5 Shift Registers

- Shift Register
  - A register capable of shifting its binary information in one or both directions
  - The logical configuration of a shift register consists of a chain of flip-flops in cascade
  - The simplest possible shift register uses only flip-flops : ***Fig. 2-8***
  - The ***serial input*** determines what goes into the leftmost position during the shift
  - The ***serial output*** is taken from the output of the rightmost flip-flop

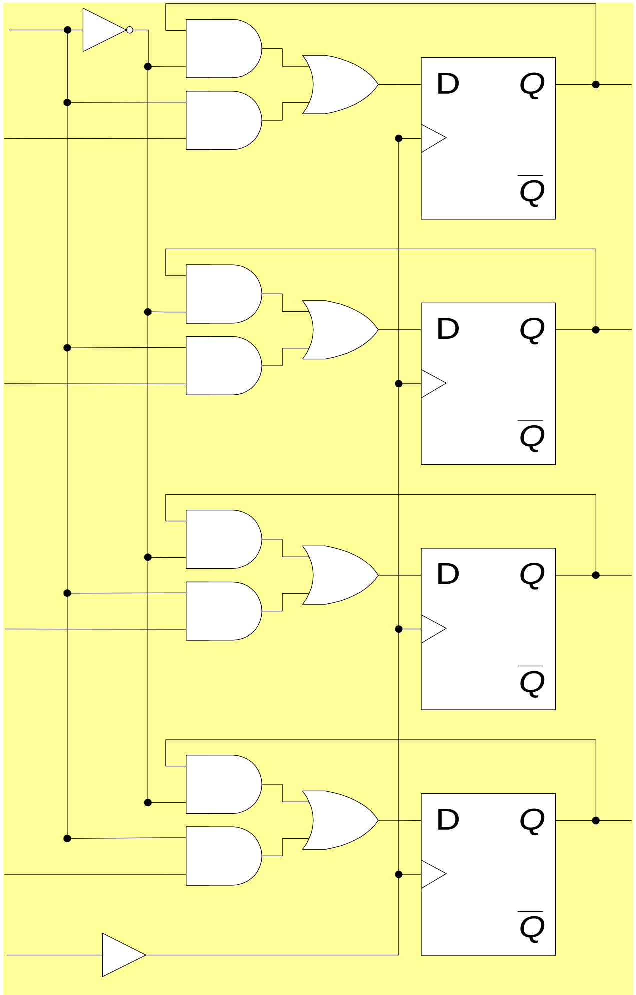


Fig. 2-8 4-bit shift register

Fig. 2-7 4-bit register with parallel load

Bidirectional Shift Register with Parallel Load

- A register capable of shifting in *one direction only* is called a ***unidirectional shift register***
- A register that can shift in *both directions* is called a ***bidirectional shift register***
- The most general shift register has all the capabilities listed below:
  - An input clock pulse to synchronize all operations
  - A shift-right /left (serial output/input)
  - A parallel load, n parallel output lines
  - The register unchanged even though clock pulses are applied continuously
- 4-bit bidirectional shift register with parallel load : ***Fig. 2-9***
  - 4 X 1 Mux = 4 , D F/F = 4

Mode		Operation
S1	S0	
0	0	No chage
0	1	Shift right(down)
1	0	shift left(up)
1	1	Parallel load

Tab. 2-4 Function Table for Register of Fig. 2-9

Fig. 2-9 Bidirectional shift register

2-6 Binary Counter

- Counter
  - A register goes through a predetermined sequence of state(Upon the application of input pulses)
  - Used for counting the number of occurrences of an event and ***useful for generating timing signals to control the sequence of operations*** in digital computers
  - An n-bit binary counter is a register of n flip-flop(count from 0 to 2^n -1)
- 4 bit Synchronous Binary Counter

J	K	Q(t+1)
0	0	Q(t)
1	1	Q(t)'

  - A counter circuit will usually employ F/F with complementing capabilities(T and J-K F/F)
  - 4 bit Synchronous Binary Counter :

Fig. 2-10

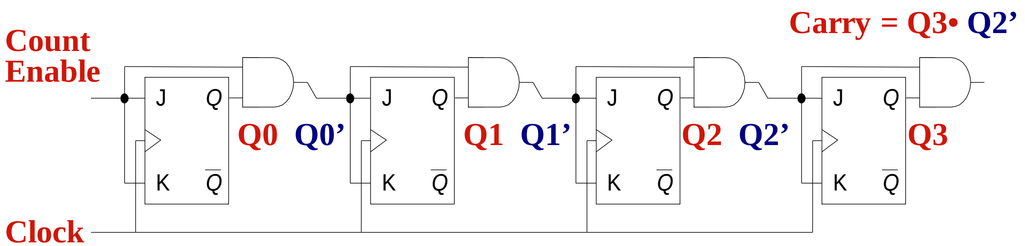


Fig. 2-10 4-bit Synchronous binary counter

Binary Counter with Parallel Load

- Counters employed in digital systems(***CPU Register***) require a parallel load capability for transferring an initial binary number prior to the count operation
- 4-bit binary counter with Clear, Parallel Load, and Increment(Counter) :

  Fig. 2-11
- Function Table : ***Tab. 2-5***

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)'

- Clear : 1 → K=X, J=0 → Clear(Q=0)
  (Clear, Load=X)
- Load : 1 (Clear=0)
  - I=1 → J=1, K=0
  - I=0 → J=0, K=1
- Increment : 1 → J=K=1(Toggle)
  (Clear, Load=0)

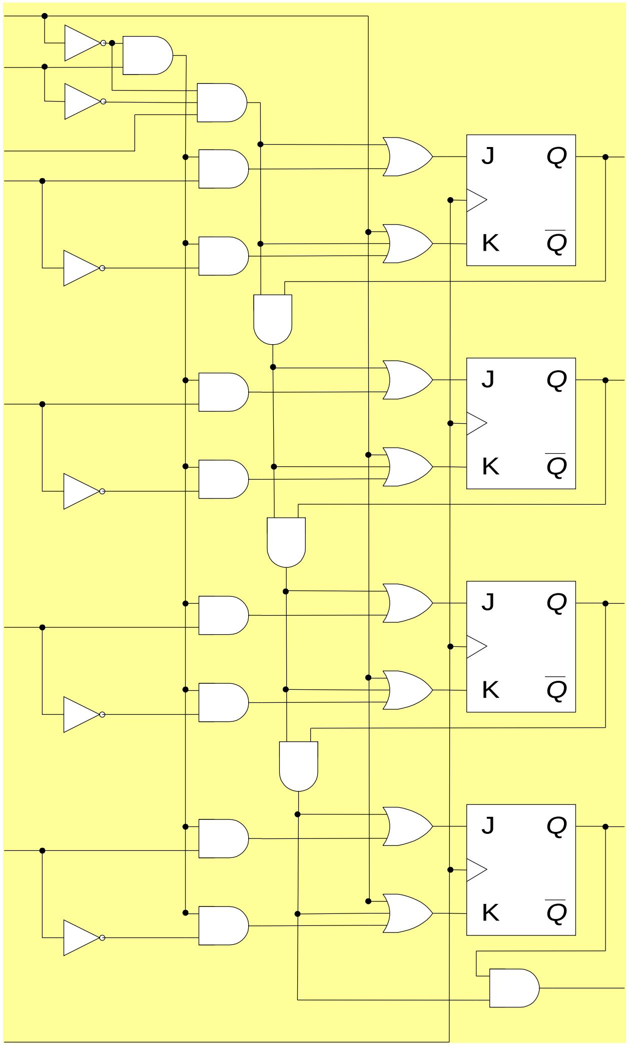
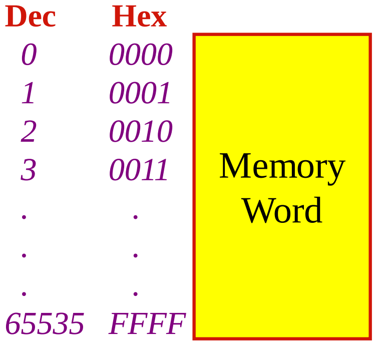


Fig. 2-11 4-bit binary counter with parallel load

2-7 Memory Unit

- Memory Unit
  - A collection of storage cells together with associated circuits needed to transfer information in and out of storage
  - The memory stores binary information in groups of bits called ***words***
  - Word
    - A group of binary information that is processed in one simultaneous operation
  - Byte
    - A group of eight bits (nibble : four bits)
  - The number of address line = k
    - Address(Identification number) : 0, 1, 2, 3, … up to 2^k -1
    - The selection of specific word inside memory : k bit binary address
    - 1 Kilo= 2^{10}, 1 Mega= 2^{20}, 1 Giga= 2^{30}
    - 16 bit address line : 2^{16}= 64 K
  - Solid State Memory(IC Memory)
    - RAM(Volatile Memory)
    - ROM(Non-volatile Memory)



Dec	Hex
0	0000
1	0001
2	0010
3	0011
.	.
.	.
.	.
65535	FFFF

- Random Access Memory
  - The memory cells can be accessed for information transfer from any desired random location
  - Communication between a memory and its environment is achieved through ***data input and output lines, address selection lines,*** and ***control lines*** : ***Fig. 2-12***
  - The two operations that a random-access memory can perform are the ***write*** and ***read*** operations
  - Memory Write
    1) Apply the binary address
    2) Apply the data bits
    3) Activate the write input
  - Memory Read
    1) Apply the binary address
    2) Activate the read input
       - » The content of the selected word does not change after reading
  - NV-RAM : battery back-up CMOS RAM

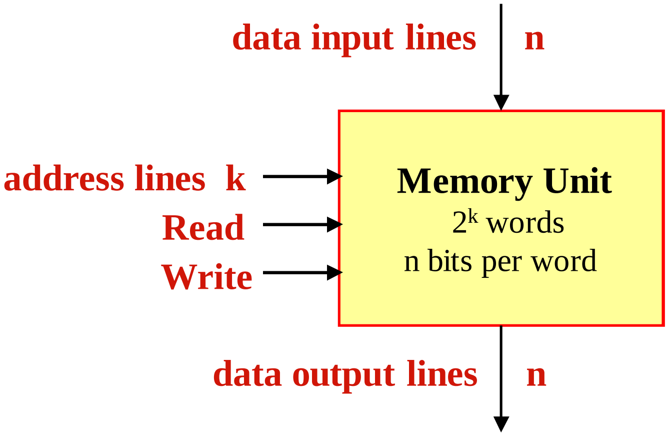
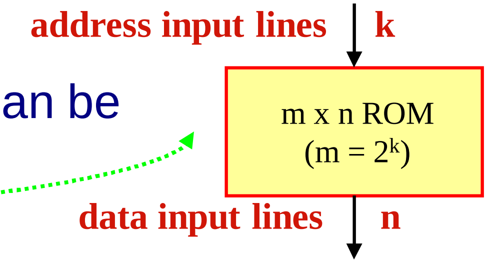


Fig. 2-12 Block diagram of RAM

- Read-Only Memory
  - A memory unit that performs the read operation ***only***; it does not have a write capability
  - ROM comes with special internal electronic ***fuses*** that can be "***programmed***" for a specific configuration
  - m x n ROM : ***Fig. 2-13***
    - k address input lines to select one of 2^k = *m words* of memory, and n output lines(n bits word)



  - ROM is classified as a ***combinational circuit***, because the outputs are a function of only the present inputs(address lines)
    - There is no need for providing storage capabilities as in a RAM
  - ROM is also employed in the design of ***control units*** for digital computers
    - A Control Unit that utilizes a ROM to store binary control information is called a ***micro-programmed control***
  - Types of ROMs
    - UVEPROM(Chip level erase), EEPROM(Byte level erase), Flash ROM(Page or block level erase), OTPROM, Mask ROM